REMARKS

In an Office Action mailed June 29, 2004, claims 8-15, 17-22 and 24-31 are pending and were each rejected. In response, Applicants have amended claims 8, 11, 13, 14, 18, 20-22, 24-26, 28, 29 and 31, canceled claims 9 and 27, and are requesting reconsideration of the rejection and the allowance of the application. Applicants thank the Examiner for a thorough, quality examination response.

Figure 1 was required to be corrected to include a "Prior Art" legend. In response, Applicants are submitting with a separate cover letter a substitute sheet 1 of 4 of formal drawings wherein Figure 1 is amended to include the required amendment. Applicants request that the drawing objection be withdrawn. Additionally, correction of FIG. 5 on sheet 3 of 4 is requested. In particular, correction of the drawing to be consistent with the written specification at page 11, lines 13-15 and the claims is requested. Step 86 should illustrate whether a set or a plurality of final value conditions (plural) are satisfied rather than a single final value condition being satisfied. Similarly, step 90 should illustrate whether a set or a plurality of initial value conditions (plural) are satisfied rather than a single initial value condition being satisfied. Applicants request approval and entrance of the drawing amendment.

Claim 11 and claim 21 were deemed to be of substantially duplicate scope. With the amendment to claim 11 herein, claims 11 and 21 are not substantially duplicative and thus should no longer be subject to an objection under 37 CFR 1.75.

Claim 24 was objected to for the use of "capable of". In response, claim 24 is herein amended to remove the phrase. With this correction, the objection to claim 24 is believed to be overcome.

Claims 13-15, 17-20 and 24-31 were rejected under 35 U.S.C. 112, first paragraph, in connection with the claim recital of the disclosed ATPG tool having an ATPG model. In response, reference to an ATPG model is removed from each of claims 13-15, 17-20 and 24-31. Therefore, withdrawal of the rejection of claims 13-15, 17-20 and 24-31 under 35 U.S.C. 112, first paragraph, is herein requested.

Claims 14, 18 and 24-31 were rejected under 35 U.S.C. 112, second paragraph for specifically stated reasons. In claims 14 and 25, the term "translating" was deemed unclear in connection with "translating the first set of paths". Applicants specification at page 10, lines 16-24, describe a translation of a path from a timing domain format into a format that can be used with commands from the ATPG tool. Therefore, claims 14 and 25 are herein amended to recite translating a first set of paths from "a first format to a second format" consistent with the written specification. Withdrawal of the stated rejection of claims 14 and 25 is therefore requested. Claim 18 was rejected in connection with the phrase "static analysis tool". In response, claim 18 is herein amended to recite a "timing analysis tool" consistent with the terminology used in the written specification such as at page 8, lines 4-6. Claims 24 and 29 are similarly amended regarding this same terminology. Therefore, the withdrawal of the stated rejection of claim 18 is requested. Claim 24 was rejected since the specification is not specifically directed toward disclosing a method for interfacing between two tools. As amended herein, the preamble of claim 24 recites that the method is for identifying false paths of a circuit design. Therefore, Applicants request withdrawal of the stated rejection of claim 24.

Claims 8-15, 17-22, 24-31 were rejected under 35 U.S.C. 102(b) as being anticipated by Kunda et al. (U.S. Patent 5,675,728). The subject matter of the Kunda et al. patent relates to identifying false timing paths. In integrated circuit

design, multiple circuit paths are checked to determine whether or not a logic value transition on the input to a circuit path will trigger a logic value transition on the output of the path. If an input does transition the output in a time duration exceeding a predetermined maximum limit, then an attempt is made to shorten the path length in an effort to increase the speed of operation of the circuit. However, this is an inefficient process that costs both a significant amount of time and money. In case an input transition can never trigger an output transition, then the path is deemed as "unsensitizable" or "false". False paths need not be shortened as they do not affect speed of operation of the circuit.

As amended herein the previously rejected claims readily distinguish from the Kunda et al. circuit. Kunda et al. do not teach or suggest "determining whether a set of final value conditions are satisfied" as recited in claim 8. Kunda et al. do not teach or suggest "determining whether a set of initial value conditions are satisfied" as recited in claim 8. Kunda et al. do not teach or suggest "determining whether a set of slower path conditions is satisfied" as recited in claim 8. Rather Kunda et al. only uses a set of side value propagation conditions and uses an ATPG tool to check the testability of the value (whether an intended value exists) at the output of the monitor circuit taught therein. At Col. 4, lines 26-29, Kunda et al. teach that the ATPG tool is used to find which vector causes the output monitor circuit to be a "1". The Kunda et al. ATPG tool is not functioning to determine whether a set of conditions is satisfied as recited in the claims, but rather is looking to determine whether a stuck-at-zero fault can be detected at the output of a circuit. Further, Figure 5 of the Kunda et al. circuit clearly illustrates that only side value propagation conditions are used. For example, an illustrated path in Figure 5 starts with the IN signal and goes through gate 1, gate 2, gate 3, and gate 6. For each gate, an associated gate monitor circuit is added. Each gate monitor circuit receives a side signal that is not in the path. The output of each gate monitor

circuit is coupled to an AND path monitor whose output is checked for an anticipated value by an ATPG tool. Multiple AND path monitors are logically ORed by monitor 517. Figure 2, as described in Col. 2 of Kunda et al., illustrates how a netlist having the gate monitors is created in the false path preparation 205 and how the ATPG tool tests the monitor output to determine if a false path exists. Note that the Kunda et al. circuit does not use any timing information and thus is unable to determine "whether a set of slower path conditions is satisfied". This lack of consideration of slow paths may result in erroneous false path determination by the Kunda et al. circuit. For example, if a path being checked by the Kunda et al. circuit is one of two inputs to a logic gate for receiving a signal that has delay associated with it with respect to the other input's signal, the output of the gate will transition differently depending upon the relative timing of the signals to the logic gate that is determined by path delay. Without this timing information, the true characterization of a path as false cannot be ensured. Another point of interest is that for each gate in the Kunda et al. circuit, a gate monitor circuit is created and for each path an AND gate monitor circuit is created. For an advanced commercial integrated circuit, the number of gates and paths can approach one billion. Therefore, the Kunda et al. circuit is not practical to implement, in addition to having the functional disadvantage of erroneous false path determinations being possible. In addition, the Kunda et al. circuit is intrusive by requiring re-routing of circuitry and the addition of circuits that add new circuit paths that modify the circuit model. In contrast, the methods recited herein recognize circuit false paths in a non-intrusive fashion and reduce a wasteful expenditure of expensive optimization time. The methods recited herein eliminate the creation of unnecessary circuit area, the dissipation of additional power and avoid reduction in circuit performance.

With respect to claim 11, Kunda et al. do not teach or suggest "determining during a first time frame whether a set of final value conditions are satisfied". Further, Kunda et al. do not teach or suggest "determining during a second time frame different from the first time frame whether a set of initial value conditions are satisfied".

With respect to claim 13, Kunda et al. do not teach or suggest using a set of conditions corresponding to a path where "the set of conditions comprising whether a final value condition is satisfied, whether one or more side value propagation conditions are satisfied, whether an initial value condition is satisfied and whether one or more slower path conditions are satisfied".

With respect to claim 18, Kunda et al. do not teach or suggest the use of a "timing analysis tool" and use of a set of conditions corresponding to a circuit path where "the set of conditions comprising determining whether one or more slower path conditions are satisfied".

With respect to claim 21, Kunda et al. do not teach or suggest the use of a path having final value conditions and initial value conditions and "determining whether a set of final value conditions are satisfied" and "determining whether a set of initial value conditions are satisfied".

With respect to claim 24, in addition to Kunda et al. not teaching the determination of satisfying final value and initial value conditions, Kunda et al. do not teach "using information from the timing analysis tool to determine whether the set of slower path conditions is satisfied".

Therefore, Applicants respectfully request the reconsideration of and the withdrawal of the rejection of claims 8, 10-15, 17-22, 24-26 and 28-31 under 35 U.S.C. 102(b). Applicants request the allowance of claims 8, 10-15, 17-22 and 24-26 and 28-31, as amended herein.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references. In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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Law Department
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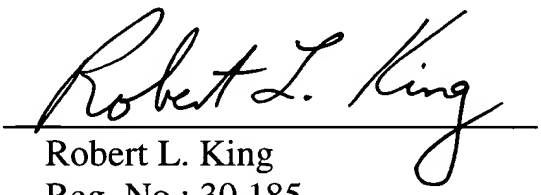
By: 

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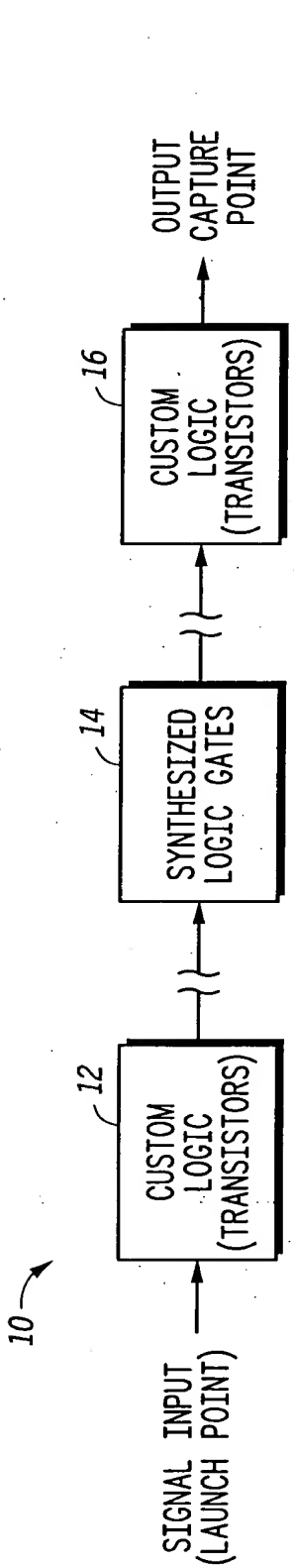

FIG.1
-PRIOR ART-

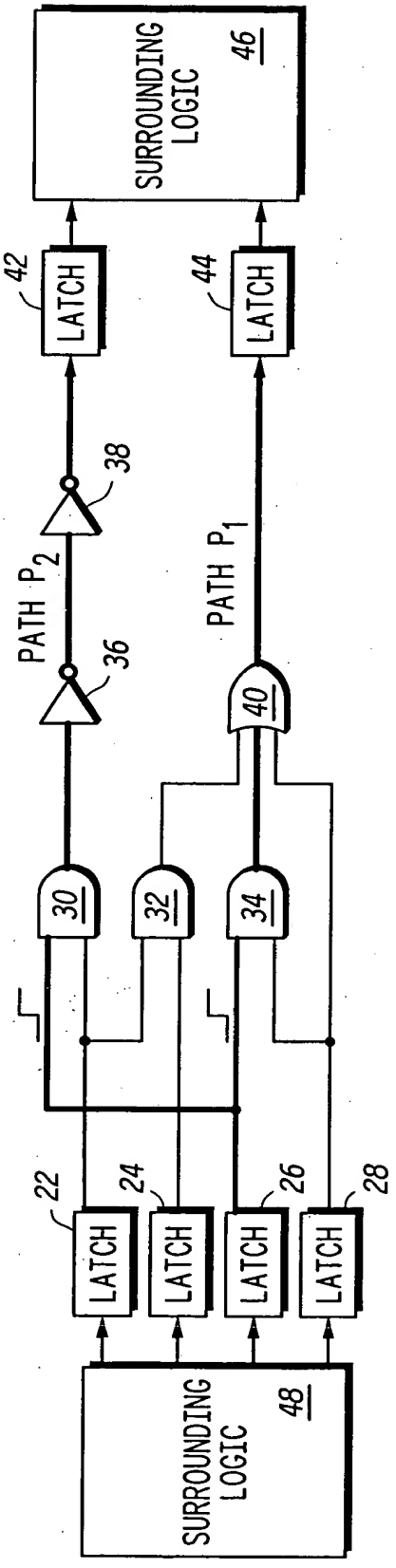

FIG.2

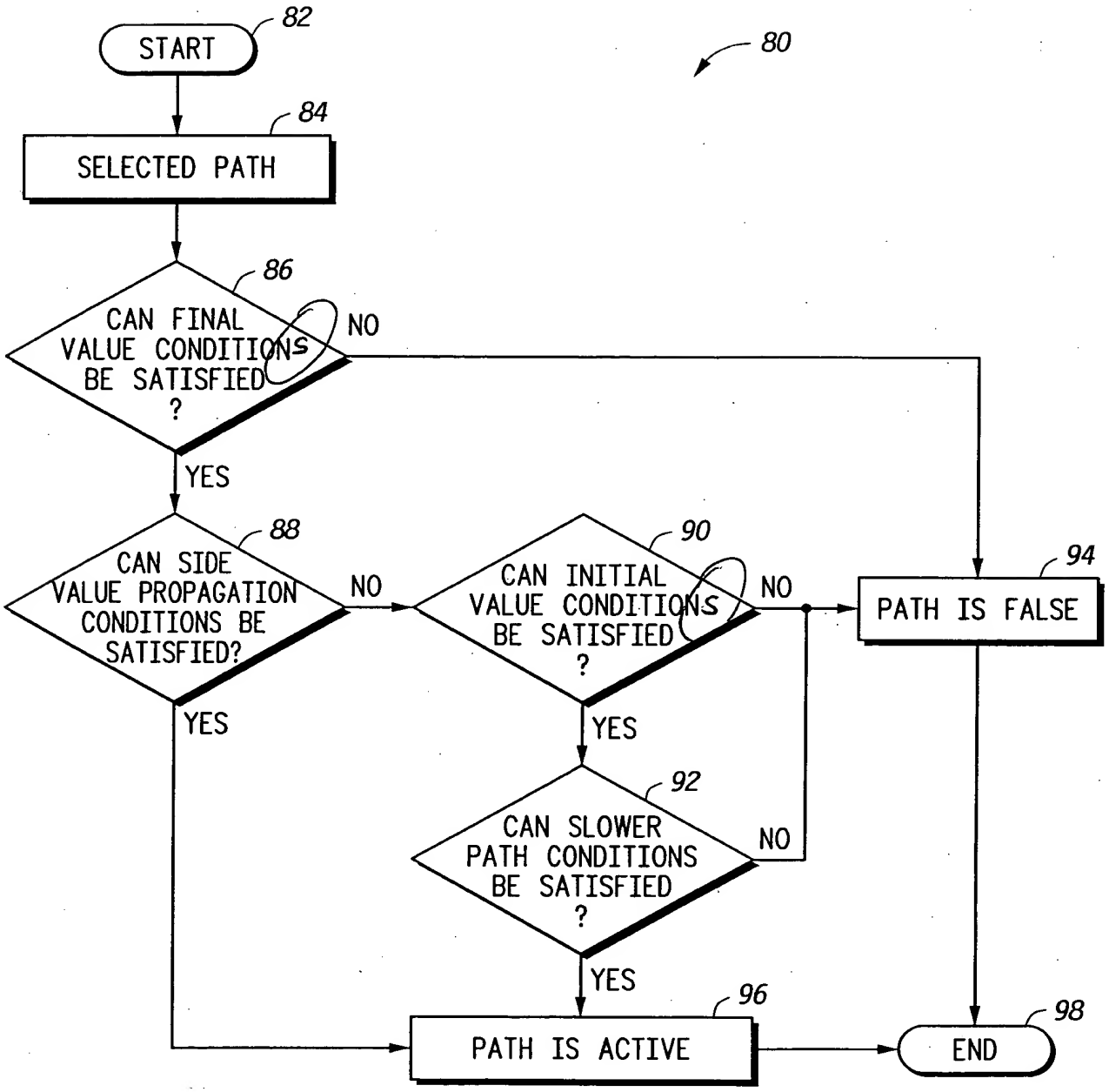

FIG.5